Behavorial Model of Carbon Nanotube Programmable Resistors

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Abstract—Hybrid Nano (e.g. Nanotube, Nanowire) /CMOS circuits combine both the advantages of Nano-devices and CMOS technologies; they have thus become one of the most promising candidates to relax the intrinsic drawbacks of CMOS circuits beyond Moore’s law. A behavioral simulation model for an hybrid Nano/CMOS design is presented in this paper. It is based on Optically Gated Carbon NanoTube Field Effect Transistors (OG-CNTFET), which can be used as 2-terminal programmable resistors. Their resistance can be adjusted precisely, reproducibly and in a non-volatile way, over three orders of magnitude. These interesting behaviors of OG-CNTFET promise great potential for developing the non-volatile memory and neuromorphic adaptive computing circuits. The model is developed in Verilog-A language and implemented on Cadence Virtuoso platform with Spectre 5.1.41 simulator. Many experimental parameters are included in this model to improve the simulation accuracy.

Keywords- Behavioral Modelling, Carbon Nanotube, Hybrid Nano/CMOS circuits, OG-CNTFET, Verilog-A

I. INTRODUCTION

Nano-devices presenting compatible interface with CMOS technology (e.g. Nanotube and memristor) [1-4] are of great interest to relax the intrinsic drawbacks of CMOS technology and improve furthermore the circuit performances beyond the Moore’s law. The hybrid Nano/CMOS circuits promises to combine both the advantages of Nano-devices and CMOS technology [3]. In order to develop hybrid circuits and architectures, a behavioral spice simulation model of Nano-devices is required as it can provide the interface between the physical behaviors of the nano-devices and electrical test-bench. Furthermore, its high accuracy is crucial for the hybrid Nano/CMOS simulation. As the CMOS transistor behaviors are well known, the design strategy for hybrid Nano/CMOS circuits is to conceive the suitable CMOS circuits for the nano-devices and then provide creditably high performance. By using the behavioral model and CMOS design kit, we can extrapolate and predict the performance of realistic hybrid circuits and architectures comprising large numbers of nano-devices.

II. BEHAVIORAL MODEL OF OG-CNTFET FOR HYBRID CIRCUIT DESIGN

A. Physical structure of OG-CNTFET and its spice symbol

There are four terminals in the OG-CNTFET (see Fig.1), Drain (D), Source (S) and Gate (G) as the conventional CNTFET [4] and an additional Optical Gate (OG) allowing the electrons to be trapped below the nanotube mats. In practical applications, the terminals G and OG are shared by a number of OG-CNTFETs. The other two terminals D, S form the tunable resistance $R_{DS}$, which can be adjusted precisely, reproducibly and in a non-volatile way, over three orders of magnitude.

![Physical structure of an OG-CNTFET](image)

Figure 1. (a) Physical structure of an OG-CNTFET composed of four terminals: Drain (D), Source (S), Gate (G) and Optical Gate (OG) (b) Symbol of OG-CNTFET in the schematic editor of Cadence.

This work is partially funded by the European Union through the FP7 Project NABAB (Contract FP7-216777) and by the French National Research Agency (ANR) through the Panini Project.


Figure 2. (a) Equivalent circuit of the OG-CNTFET from the “off” to “on” state, R_A and R_B are tunable resistance and depend dynamically on the duration of the laser pulse. (b) Equivalent circuit from “on” to “off” state, R_B depends only on the drain voltage and R_A varies dynamically with the drain and gate voltages.

Based on the switching behaviors of OG-CNTFET, equivalent electrical circuits have been implemented in the model (see Fig.2). R_0 and R_1 representing the R_on are constants obtained from the experimental measurement. R_A and R_B are tunable resistances from 0 to R_off. V_{OG}, n and t represent the wavelength of laser, number of pulses and the pulse duration respectively.

This behavior model provides high flexibility for hybrid Nano/CMOS design; V_D configuration can be changed to get desired results. For example by lowering the pulse duration, more resistance states can be obtained thus improving the circuit precision; by increasing the V_D amplitude, less resistance states are obtained but the circuit speed can be accelerated. The best design is a tradeoff between speed and precision and is obtained with the most suitable V_D.

Spice simulations have been performed after the implementation of the electrical equivalent circuit in the Verilog-A model. Fig.3 shows the programmable resistivity of OG-CNTFET driven by both the laser (from R_off to R_on) and V_D (from R_on to R_off). Fig.4 shows different reset paths of an OG-CNTFET led by the three V_D amplitudes. This effect can be explained by the resistivity (R_B) during the reset path (see Fig. 2b), which depends only on V_D amplitude.

C. Random initial effect for each OG-CNTFET

The small dimension of nanocomponents and their self-assembly fabrication process leads to important intrinsic mismatch variation, which could have critical influences on the circuits and architecture design [7]. Thereby the random initial effect has been taken into account in the behavioral model (see Fig.5). Based on our experimental data, the random initial state of different OG-CNTFETs is found to follow approximately the Gaussian distribution and the resistance variation can be attained up to 25%.

Figure 3. Spice simulation of OG-CNTFET functional model. Three laser pulses (red flashes) are used here to drive it from “off” to “on” state. The V_D pulses (100ms@6V) reset the OG-CNTFET from “on” to “off” state.
III. FROM A SINGLE OG-CNTFET MODEL TO A SMALL CIRCUIT ARCHITECTURE

A small architecture composed of 4 OG-CNTFETs has been simulated, in which all the OG-CNTFETs share the same OG and G terminals. As a result, four two-terminal tunable resistors are formed. They can be programmed globally by the OG and G terminals and each OG-CNTFET can be also tuned individually by the D terminals (see Fig.6). The terminals S are also connected together to sum the currents from the four resistors.

Based on the small architecture, a new symbol is created to simplify the hierarchy design and simulation. Figure 7 and Figure 8 show respectively the electrical test-bench and simulation for the basic architecture. As shown on figure 8, an arbitrary number of resistor levels can be realized. This has a direct effect on the data processing precision. Several basic 4 element circuits can be hierarchically combined in order to build more complex architectures and simulate them.

IV. CONCLUSION

This paper introduces a behavioral model of OG-CNTFET for hybrid Nano/CMOS design; it includes the dynamic behaviors, random initial effect and a number of experimental parameters. The structure of this behavioral model could be easily used to develop the models for other two-terminal programmable nano-components such as Memristor [2] and CBRAM [5] and NOMFET [8] etc. Based on this model and CMOS 65nm design kit [9], hybrid neuromorphic circuits comprising nanoscale synapses and CMOS neurons can be realized [10]. The memory applications of OG-CNTFET are currently under investigation in our laboratory.
ACKNOWLEDGMENT

The author would like to thank Göran Wendin and Yves Lhuillier for very fruitful scientific inputs. We also thank Mickael Guibert, Jean-Marc Philippe, Renaud Schmitt and Francis Lugiez for expert technical assistance.

REFERENCES


Figure 7. Electrical test-bench for the small architecture shown in Figure 6, a new symbol has been created to simplify the hierarchy design and simulation.

Figure 8. Spice simulation of the small architecture composed of four OG-CNTFETs, the four OG-CNTFETs have been initialized globally to “on” state by the shared Optical Gates, in the following the reset voltage pulse drive individually the four tunable resistors from “on” to “off”. Ids is the summated current at the shared S terminal.