Abstract—Emerging synapse-like nanoscale devices such as memristive devices and synaptic transistors are of great interest to inspire new circuits or systems and promise adaptability, high density and robustness. We reported recently the Nanoparticle-Organic Memory FET transistor (NOMFET), which exhibits interesting behaviors similar to a biological spiking synapse in neural network. A functional model of NOMFET is presented in this paper, which agrees well with the experimental results. It allows then the reliable conception and simulation of hybrid Nano/CMOS circuits. The model is developed in Verilog-A language and implemented on Cadence Virtuoso platform with Spectre 5.1.41 simulator. An iterative physical model and a number of experimental parameters have been integrated to improve the simulation accuracy.

I. INTRODUCTION

CMOS Neuromorphic circuit was one of the most intense researches to bring adaptability and robustness in circuits beyond the conventional Von Neumann architecture in early 1990’ [1-3]. However, CMOS technology could not provide the huge capacity to be scalable to biological levels because a great number of transistors are required to emulate the dynamic behaviors of biological synapses [4]. This approach was nearly suspended until 2 or 3 years ago when nanoscale components such as memristive devices and synaptic transistors where demonstrated [5-9]. They are of great interest to develop new neuromorphic circuits and architectures by replacing CMOS based synapses, but keeping CMOS based neurons [10-11]. The Nanoparticle–Organic Memory FET transistor (NOMFET), shown in Fig.1, is a promising candidate as it can exhibit dynamic behaviors similar to a biological spiking synapse [12-13]. Thus it could be very suitable to implement some dynamic neural network based computing systems such as the liquid state machine [14] and some natural synaptic learning mechanisms such as Spike-Timing-Dependent Plasticity (STDP) [15].

In order to design and simulate the hybrid neuromorphic circuits or architectures composed of nanocomponent as synapses and CMOS as neurons, a reliable spice model is required to provide the interface between the fundamental physics and electrical characteristics. Therefore we developed a functional model based on a physical model and a number of experimental parameters. It is more accurate than a purely mathematical model, much faster than a compact model [16] for architecture simulation and easier to be updated. Different from the conventional methods for static devices, special methods and techniques such as data fitting, parameter extraction and simulation processing have been developed for the modeling of dynamic behaviors in pulse regime, which could be extended to develop the functional model of other nanoscale memristive devices as well.

The body of this paper includes four parts. In the first section, the NOMFET and its synapse-like behaviors are briefly introduced. In the following, a functional model based on the physical mechanisms occurring in the device is derived; the methodology to extract the model parameters from experimental data is detailed in the third part. Finally, the Verilog-A [17] implementation of the model in the IC development platform Cadence Spectre [18] is then presented, along with the spice simulation results.

II. DEVICE CONFIGURATION

The NOMFET is composed of three terminals as the conventional MOSFET (see Fig. 1), Drain (D), Source (S) and Gate (G). It is fabricated using a bottom-gate electrode...
configuration, where the p+ doped silicon gate is covered with 200 nm of SiO₂. The terminals D and S are gold electrodes with inter-electrode gap in the range 0.2 - 20 µm. Gold NanoParticles (NP, diameters of 5, 10 or 20 nm) are immobilized on the surface of the inter-electrode gap by surface chemistry before pentacene deposition. The pentacene is a p-type organic semiconductor [12-13]. The electrical conduction between the terminals D and S is assured by the holes’ channel, which is created in the thin film at the interface with the silicon oxide by applying a negative gate voltage. The drain to source current $I_{DS}$ is negative. In addition to classical transistor’s behaviors, a negative gate voltage also positively charges the Au NPs. This reduces the channel conductivity of the device, because the charged NPs induce a repulsive electrostatic interaction between the holes trapped in the NPs and the ones in the pentacene channel. The NOMFET therefore exhibits a short term memory and the charge retention time in the NPs can be as long as several thousand seconds [12].

We established our model for a two-terminal device configuration, as shown Fig. 2. The gate and the drain electrodes are driven by the same input voltage, a pulse train with amplitude $V_{AP}$ and of a variable frequency (see Fig. 3). In this configuration, the dynamic behaviors of the NOMFET are similar to a biological spiking synapse [13]. There is a competition between the charges provided to the NPs by the gate voltage pulses and the natural NPs charge relaxation. They can result in a decrease and increase of $I_{DS}$ respectively. When a new input pulse sequence occurs, the NOMFET exhibits either a depressing or a facilitating behavior, depending both on the duration between the pulses and on the charge level of the NPs. The current $I_{DS}$ is thus dependent on the history of the input signal and its maximum variation on our devices is close to 25% with -30 V pulses amplitude. New samples with 200 nm gap and 5 nm NPs diameter exhibit similar behaviors with a drive voltage as low as -3 V and the current variation could be improved up to 80% with a new device configuration.

III. FUNCTIONAL MODEL DERIVATION

The model integrates both the effects of the charges trapped in the NPs on $I_{DS}$ and the NPs (dis)charge dynamics. The current in the device is determined using the expression proposed in [13]:

$$I_{DS} = \sigma V_{DS}$$

with

$$\sigma = A_0 e^{\beta \Delta - \beta \Delta},$$

$$\beta = 1/(k_B \theta),$$

$\theta$ is the temperature, $A_0$ is a temperature dependent parameter, $e_F$ is the Fermi energy fixed by the gate voltage and $\Delta$ is the shift of the Fermi energy induced by the charges trapped in the NPs. For a given bias, a simplified form can be obtained for (1)

$$I_{DS} = \bar{I} e^{-\beta \Delta}$$

$\bar{I}$ is the current between the terminals Drain and Source when the NPs are fully discharged. This expression is coherent with the physical interpretation mentioned in the previous section.

A. Iterative model derivation

The input waveform applied to the device is illustrated in Fig. 3. $I_n$ is the drain-to-source current at the n-th pulse. From $t_n$ to $t_{n+} = t_n + W$ (pulse width), the negative voltage $V_{GS}$ charges the NPs. The charges follow a certain dynamic characterized by an empirical function $f_c(t)$ (6). Taking its value from 1 to 0. For an infinite pulse width, the NPs tend to be charged completely, inducing a maximum Fermi energy shift $\Delta_{\text{max}}$. The expression of the current at $t = t_{n+}$ is

$$I_{n+} = I_{n} f_c(W) + \bar{I} e^{-\beta \Delta_{\text{max}}}(1 - f_c(W)).$$

From $t_{n+}$ to $t_{n+1} = t_n + T$, the charges trapped in the NPs are relaxed and the current intensity ultimately tends to $\bar{I}$. As for the charge, the relaxation dynamic is described by another empirical function $f_D(t)$.

$$I_{n+1} = I_{n+} f_D(T-W) + \bar{I} (1 - f_D(T-W)).$$

The general iteration expression for the evolution of the current $I_{DS}$ between two pulses can be obtained by integrating (3) into (4):

$$I_{DS} = \sum_{n} I_{n+}$$
Figure 4. Steady state current calculated from the model vs. experimental measurement (dots). The fitting is based on multiple sequences of constant frequency; the gap width of the NOMFET is 12 μm and the size of the NPs is 5 nm. W is fixed to 200 ms and T varies from 200 ms to infinite. The steady state current is -7.5 nA as the NPs are fully charged whereas the current is -7.5 nA as there is no charge in the NPs.

\[
I_{n+1} = I_n \cdot f_C(W) \cdot f_D(T - W) + I \cdot e^{-\beta \Delta_{\text{max}} \cdot (1 - f_C(W))} \cdot f_D(T - W) + 1 - f_D(T - W) \]

(5)

B. NPs charge/discharge dynamic behaviors

By introducing two time constants \( \tau_C \) and \( \tau_D \) in the model, a simple exponential function can be used as \( f_C(t) \) and \( f_D(t) \) in (3-5), which is sufficient to simulate the (dis)charge dynamic behaviors with good accuracy.

\[
f_C(t) = e^{-t/\tau_C} , \quad f_D(t) = e^{-t/\tau_D} .
\]

(6)

C. Current expression in steady state \( I_\infty \)

Considering the limit of (5) for an infinite number of iterations with given pulse width and frequency, one gets the current intensity expression of a steady state

\[
I_\infty = \int I \cdot e^{-\beta \Delta_{\text{max}} \cdot (1 - f_C(W))} \cdot f_D(T - W) + 1 - f_D(T - W)
\]

(7)

If \( T = W, f_D(T - W) = f_D(0) = 1 \), the NPs are continuously charged. When the full charge capacity of the NPs is reached, \( I_\infty = I \cdot e^{-\beta \Delta_{\text{max}}} \). On the contrary, if \( T \gg W \), the NPs are totally relaxed between each pulse and \( I_\infty = \bar{I} \). Fig. 4 shows a comparison between the steady state current calculated from the model and the measured data in function of the pulse frequency. There is a good agreement between the two curves.

IV. MODEL PARAMETER EXTRACTION

Our model integrates the four physical parameters introduced above: the NPs charge and discharge time constants, \( \tau_C \) and \( \tau_D \), the maximum Fermi energy shift \( \Delta_{\text{max}} \) and \( \bar{I} \), which depends mainly on the bias of the device. Several experimental measurements of the current response for voltage pulse sequences with a variable frequency are used to fit the model. The Non-Linear Curve Fit toolset of OriginPro 8.0 and OriginC programming language are used for the data fitting. They allow the use of static variables to fit the experimental data directly with the iterative function (5). Since there are less experimental data for low frequency pulses than for higher ones during the same time interval, a weight inversely proportional to the pulse frequency is attributed to each data. This ensures that equal importance is given to each part of the pulse sequence for the fitting, regardless of the frequency.

V. IMPLEMENTATION AND SIMULATION RESULTS

The iterative electrical model is implemented in the Verilog-A hardware description language [16], which can be incorporated directly into the Cadence Spectre circuit simulator. It allows the designers to predict the performance of NOMFET by using the electrical test-bench and to simulate the hybrid circuits with other components (e.g. MOS transistors). In our implementation, the current \( I_{\text{DS}} \) is calculated at the beginning of each pulse. It depends on \( W \) and \( T \), which are computed by measuring the time at falling and rising edges of each pulse during the simulation: \( T = t_{n+1} - t_n \) and \( W = t_{n+1} - t_n \) (see also Fig. 3). The other parameters are those extracted directly from the data fitting.

Transient simulation of NOMFET for a pulse train sequence is shown in Fig. 6. It shows a good matching with the experimental data. It is important to note that the depressing and facilitating synaptic behaviors can be observed, which depend on both the frequency and the historical current level. The 1 Hz sequence is a good example to demonstrate this behavior: the weight or resistance of the NOMFET can increase or decrease depending on its previous states. A test-bench circuit for the NOMFET in the Cadence Spectre 5.1.41 CAO platform [17] is shown in Fig. 5. The input pulse sequence voltage is generated using a simple piecewise linear voltage source. The NOMFET symbol allows hierarchical design and hybrid circuits with CMOS transistors can also be easily conceived and simulated.

Complementary to the Cadence Spectre simulator, Matlab is used to generate hybrid nano/CMOS circuit netlist and handle the simulation results. It is indeed suitable to generate complex pulse voltage sources in an automated way through netlist manipulation and it is also a powerful tool to perform signal analysis on simulated data. The Spectre Toolbox dedicated for Matlab provides the required interface for reading simulation results in Matlab.
Figure 6. The transient simulation of the functional model shows a good agreement with the experimental measurements (inset). The same input pulse train sequences are used for the experimental measurement of the drain-to-source current response of the NOMFET (12 μm gap width, 5 nm NPs size) with a variable frequency (0.05 Hz – 3 Hz). Depending on the historical weight or current level, depressing and facilitating behaviors can be observed for the same frequency (e.g. 1 Hz).

VI. DISCUSSION AND CONCLUSION

This paper introduces a spice model of the NOMFET in pulse regime for hybrid Nano/CMOS design. It is fully functional to simulate the dynamic behavior of the NOMFET as a spiking synaptic device. The implementation in Verilog-A allows the model to easily integrate new experimental results. Different simulations have been performed on different devices (with different gap width and NPs size) and have shown a good agreement with the experimental measurements. Furthermore, in order to increase the simulation capacity of the model, the classical FET equations could be integrated in this model to compute the parameter $\tilde{I}$ in linear and in saturation regimes. It would require a few additional experimental parameters such as the carrier mobility in pentacene or the length of the conduction channel. The special methods and techniques that we developed can be very useful to study other memristive nanodevices.

Hybrid NOMFET/CMOS neuromorphic computing circuits and architectures are currently under investigation in our laboratory and future work will include also the model refinement taking into account the mismatch variation and experimental progress, synapse-to-neuron interfacing and neuronal learning architecture simulation.

REFERENCES


