Spintronics Science has emerged in 1988 with the discovery of the Giant Magneto-Resistance (GMR) effect by Pr Fert and Pr Grünberg, for which they received the 2007 Nobel Prize. In 1991, B. Dieny patented an industrial version of the GMR effect, the Spin-Valve (SV) configuration which has been progressively introduced, since 1997, in all the Hard Disk Drives (HDDs). Spintronics Science is thus well recognized in the data storage industry and this position was recently reinforced with the introduction by Everspin of the first magnetic solid-state memory (MRAM). This new class of memory today address specific niche markets such as battery backed SRAM but its high level performances combined with a high resistance to harsh environment make it also attractive for space, nuclear or aeronautic markets. Beyond data storage industry, Spintronics Science can propose disruptive technologies that could offer discriminating benefits over classical CMOS counterparts. However, they suffer from quite a dogged industrial mistrust partly due to the “complexity” of this science, to contamination concerns when handling so many unusual materials and to the lack of pre-industrial prototypes with high level of integration.

For instance, Most of the field-programmable gate arrays (FPGAs) are currently SRAM based. The possibility to stack the MRAM over the CMOS logic in a single chip and to store permanently without power the configurations in Non-Volatile Magnetic FPGAs (NVM-FPGA) dramatically simplifies the system level design and integration into the final product. NVM-FPGAs do not require configuration loading at power-up or brown-out detection strategies in power glitch situations. Another attractive application is certainly for Embedded processor; this can be done in several ways. The first one is to consider that 3D integration of MRAM will facilitate integration of efficient large cache Memory connected directly with the datapathCPU. Recent experiment did by Pr. Narayana shows clearly a benefit for the ILP and power consumption. The second approach is to drive new opportunities to enhance reliability in the embedded processor area. Indeed, the fact of having a fast and low-power non-volatile technology will permanently store the intermediate state of the system. These states will be used as of redundancy or system checkpoints (for rollback mechanisms).

The objectives of this session is to demonstrate and to discuss about this disruptive technology and to show how it can be efficiently used in the future for the design (2D and 3D) of low power embedded systems and applications. The mitigation of CMOS and MRAM technology is new and open direction that the VLSI consortium should be take into account in the near future. For this special session, after a brief introduction about the potentiality of Magnetic Memory inside System On Chip, Pr. Takahiro Hanyu (RIEC, Tohoku University, Japan) will present his view about the way to design a low power FPGA Based on MTJ/MOS-Hybrid Circuitry. Nonvolatilelogic-in-memory architecture, where nonvolatile memory elements are distributed over a logic-circuit plane, isexpectedto realizeboth ultra-low-power and reduced interconnection delay. Then Pr Vijaykrishnan Narayana (Pennsylvania State University),shows how it is possible to consider STT-MRAM as a good candidate for TLB (Translation Look aside Buffer) implementation for embedded processor area. He demonstrate performance, power and area benefits by using STT-RAMS in place of or along side SRAMs. He obtained a best case performance improvement of up to 24% using the partitioned TLB scheme. He also obtained leakage energy savings of around 97% under iso-area conditions and 95% under iso-capacity conditions. This session will be closed by Dr Keizo Kinoshita (NEC, Japan), discussing on the Manufacturing issues to realize non-volatile memory & logic devices with MTJ. Different objectives will be detailed during this presentation. Those are high-speed embedded memory and large-volume stand alone memory, and each of them is replacement for embedded SRAM and flash, respectively.

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