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Perpendicular-magnetic-anisotropy CoFeB racetrack memory

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Current-induced domain wall motion in magnetic nanowires drives the invention of a novel ultra-dense non-volatile storage device, called “racetrack memory.” Combining with magnetic tunnel junctions write and read heads, CMOS integrability and fast data access speed can also be achieved. Recent experimental progress showed that perpendicular-magnetic anisotropy (PMA) CoFeB could be a good candidate to build up racetrack memory and promise high performance like high-density (e.g., ~1 F²/bit), fast-speed, and low-power beyond classical spin transfer torque memories. In this paper, we first present the design of PMA CoFeB racetrack memory and a spice-compatible model to perform mixed simulation with CMOS circuits. Its area, speed, and power dissipation performance has been simulated and evaluated based on different technology nodes. © 2012 American Institute of Physics. [http://dx.doi.org/10.1063/1.4716460]

I. INTRODUCTION

The observation of electrical current-induced domain wall (DW) motion in magnetic nanowires promises numerous perspectives1,2 and the most interesting one is to build up a novel ultra-dense non-volatile storage device, called “racetrack memory”3,4 (see Fig. 1). Write head nucleates a local domain in the magnetic stripe and a current pulse drives the domain to move sequentially from write head to read head. Data or magnetization direction are stored between two artificial potentials or constrictions, which pin the DW as no current pulse is applied. The distance between two constrictions W can be extremely small to some nanometers and this allows >GB storage in a small die. Compared to other non-volatile memory candidates,5 the scalability potential of racetrack memory is evident. By using magnetic tunnel junction (MTJ) write and read heads, its operations like domain nucleation, DW motion, and detection can be addressed directly by CMOS circuits.6 This hybrid integration makes racetrack memory promise high performance like fast-speed (>100 MHz) and low power beyond classical spin transfer torque memories (STT-MRAM). Based on in-plane magnetic anisotropy, the first racetrack memory prototype was presented recently despite of its small capacity 256 bits.7 However, the intrinsic low energy barrier E separating the two in-plane magnetization directions of storage layer leads to short data retention in advanced technology node (e.g., 22 nm).8 This limits its use for high-density racetrack memory. Perpendicular magnetic anisotropy (PMA) in CoFeB/MgO structures providing a high energy barrier E (Refs. 9 and 10) was demonstrated and PMA MTJ become one of the most promising candidates to realize a read head. Advantageous domain wall nucleation current and speed of PMA MTJ were also observed recently11 and this makes it to be a better write head than in-plane MTJ.

In this paper, we present firstly the design of PMA racetrack memory composed of CoFeB magnetic stripe and CoFeB/MgO MTJs. A spice-compatible compact model based on experimental measurements and theoretical models is secondly described to perform the numerical simulation with CMOS circuits. At last, we evaluate and analyze the performance of PMA racetrack memory including power consumption, area, and data access speed based on the spice simulation.

II. STRUCTURE DESIGN AND COMPACT MODELLING

The structure of PMA racetrack memory is shown in Fig. 2, which includes mainly three parts: a CoFeB magnetic stripe separated by constrictions to store data, two CoFeB/MgO MTJs as write and read heads, CMOS circuits generating the DW nucleation (Iw), propagation (Ip) and detection (Ii) currents. The number of constrictions equals to the number of stored bits and CMOS circuit dominates the whole area of this racetrack memory as the magnetic stripe is implemented at the back-end through 3D integration as MRAM. Fig. 3 shows one example of CMOS circuits to generate Iw and Ip, which are, respectively, bi-directional and uni-directional in the side of write head. Ii is also a uni-directional driven by a sense amplifier12 and it can convert the stored data from magnetization direction “up” or “down” to digital signal “0” or “1.” In order to achieve the best write and read reliability, the width of write and read heads are different. For writing, a lower resistance of MTJ0 with larger width can reduce the rate of oxide barrier breakdown, which is one of the most significant constraints of the high-speed STT switching mechanism. On the contrary, high resistance of the MTJ1 with smaller width for reading can greatly improve the sensing performance.12

In order to demonstrate the operations of this PMA racetrack memory, a spice compact model has been developed, which is programmed with Verilog-A language13 and compatible with standard computer-aided design (CAD) tools. It
includes mainly three physical models describing, respectively, the DW nucleation and detection in CoFeB/MgO MTJ, DW motion in magnetic stripe. A number of experimental parameters have been integrated directly to optimize its simulation precision and efficiency (see Table I).

The first physical models are dedicated to calculate the critical current $I_{C_0}$ and switching dynamics of the PMA write head, which is induced by spin-polarized current and nucleates a new DW in the magnetic stripe. $I_{C_0}$ can be expressed by Eqs. (1) and (2): \[ I_{C_0} = \frac{\gamma e}{\mu_B S_H} (\mu_0 M_S) H_K V_m = 2 \frac{\gamma e}{\mu_B S_H} E \] \[ E = \frac{\mu_0 M_S \times V_m \times H_K}{2} \] where $E$ is the barrier energy, $\gamma$ is the magnetic damping constant, $\gamma$ is the gyromagnetic ratio, $e$ is the elementary charge, $\mu_B$ the Bohr magneton, and $V_m$ the volume of the free layer. Equation (1) shows that $I_{C_0}$ is proportional to the perpendicular anisotropy field $H_K$, while the calculation of $I_{C_0}$ in in-plane anisotropy MTJ is more complex as it depends mainly on the demagnetization field $M_S$. This is the reason to explain the reduction of $I_{C_0}$ for PMA MTJ.

It is worthy to note that the spin accumulation effects are neglected in this compact model and the spin polarization efficiency factor $g$ is obtained with the following equation: \[ g = g_{sv} \times g_{tunnel} \] where the sign depends on the free-layer alignment $g_{sv}$ and $g_{tunnel}$ which are, respectively, the spin polarization efficiency in a spin valve and MTJ. They are both predicted by Slonczewski to be

\[ g_{sv} = \left[ -4 + \left( P + P^2 \right) \frac{3 + \cos \theta}{4} \right]^{-1} \] \[ g_{tunnel} = \frac{P}{2(1 + P^2 \cos \theta)} \]

where $P$ is the spin polarization percentage of the tunnel current, $\theta$ is the angle between the magnetization of the free and reference layers.

The average DW nucleation duration is presented as \[ \frac{1}{\langle \xi \rangle} = \frac{2}{C + \ln \left( \frac{\pi^2 \xi}{4} \right)} \frac{\mu_B P_{ref} P_{free}}{e M_S (1 + P_{ref} P_{free})} (I_{write} - I_{C_0}) \] where $C \approx 0.577$ is the Euler’s constant, $\xi = E/k_B T$ is the activation energy in units of $k_B T$, $P_{ref}$, $P_{free}$ are the tunneling spin polarizations of the reference and free layers, we assume that $P_{ref} = P_{free} = P$ for this compact model, $m$ is the magnetic moment of free layer.

The second physical models are dedicated to calculate DW motion speed velocity and driven current $I_p$. The velocity of DW motion in perpendicular magnetized CoFeB nanowire can be given by the following equations:

\[ V = \frac{\beta}{x} u \] \[ u = \frac{\mu_B P_i}{e M_S} \left( j_p > j_{propagation} \right) \]

TABLE I. Parameters and variables present in the fitting functions.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Default value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\tau_{ox}$</td>
<td>Oxide barrier height</td>
<td>0.85 nm</td>
</tr>
<tr>
<td>Area</td>
<td>MTJ interface surface</td>
<td>65 nm x 65 nm x $\pi$/4</td>
</tr>
<tr>
<td>TMR(0)</td>
<td>TMR ratio with 0 $V_{bias}$</td>
<td>120%</td>
</tr>
<tr>
<td>$V$</td>
<td>Volume of free layer</td>
<td>Surface x 1.3 nm</td>
</tr>
<tr>
<td>$R_A$</td>
<td>Resistance-area product</td>
<td>10 $\Omega$ mm²</td>
</tr>
<tr>
<td>$V_{write}$</td>
<td>Writing voltage</td>
<td>2 V</td>
</tr>
<tr>
<td>$V_{read}$</td>
<td>Reading voltage</td>
<td>1.2 V</td>
</tr>
<tr>
<td>$I_{nucleation}$</td>
<td>DW nucleation current density</td>
<td>$5.7 \times 10^6$ A/cm²</td>
</tr>
<tr>
<td>$I_{propagation}$</td>
<td>DW propagation current density</td>
<td>$6.2 \times 10^7$ A/cm²</td>
</tr>
</tbody>
</table>

FIG. 1. Current induced PMA domain wall propagation in a long CoFeB magnetic stripe; MTJs are used as write and read heads for nucleating and detecting the magnetization.

FIG. 2. The cross-section structure of racetrack memory. At the back-end process, the magnetic stripe is implemented above the CMOS/MTJ interfacing circuits, which generate $I_r$ for reading, $I_w$ for domain wall nucleation, and $I_p$ for domain wall propagation. There are only two contacts for each stripe.

FIG. 3. Full current induced domain wall nucleation (MN1-2, MP1-2) and propagation (MN3) schematics.
where $\beta$ is the nonadiabatic coefficient, $\alpha$ is the damping constant, and $u$ is the current velocity. As $\beta$, $\alpha$ depend on the material of the magnetic stripe, the velocity can be increased linearly with a higher current density $J_p$ or $I_p$ as $J_p$ exceeds the critical current density $J_{c,\text{propagation}}$. In the opposite case, the current cannot propagate the DW and the velocity is kept to zero. This dynamics allows the model to be used in the simulation of high-speed racetrack memory (>GHz).

The third physical models are used to detect the magnetization direction by tunnel magnetoresistance (TMR) effect. The MgO barrier tunnel resistance model and bias-voltage dependent TMR model have been integrated to read the storage data in the magnetic stripe. A simplified equation to calculate the resistance of CoFeB/MgO/CoFeB MTJ is presented in Ref. 20.

$$R_P = \frac{t_{ox}}{k \times \phi^{-1/2} \times \text{Area}} \times \exp\left(1.025 \times t_{ox} \times \phi^{-1/2}\right),$$

where $\phi = 0.4$ is the potential barrier height of crystalline MgO, $t_{ox}$ is the thickness of oxide barrier, and Area is the MTJ area (see Table I). $k$ is a factor calculated from the resistance-area ($RA$) product value of MTJ, which depends on the material composition of the three thin layers. For this model, $RA$ is defined as a parameter $= 10 \ \Omega \ \mu m^2$, which gives $k = 332.2$ with Eq. (9).

The simulation results of this compact model present good agreement (e.g., DW motion shown in Fig. 4) and high accuracy with conventional micro-magnetic simulation. Verilog-A language provides an easy interface to manage the parameters allowing the model to be expediently extended to other PMA racetrack memory structures different from CoFeB/MgO.

### III. RESULTS AND DISCUSSION

By using this spice-compatible model and STMicroelectronics CMOS 65 nm design kit, a PMA racetrack memory of 8 bits (see Fig. 2) has been successfully co-simulated. Fig. 5 shows the transient simulation results driven by 50 MHz domain wall propagation current pulse $I_p \approx 68.43 \mu A$ and its duration is 2.5 ns (see Fig. 5(b)). Initially, the states of all the storage elements in the magnetic track are set to “0” and we plan to store an arbitrary logic pattern “…00010100111000…” The pattern is firstly sent to write head MTJ0 and the domain wall nucleation current $I_w \approx 140 \mu A$ is activated during each data transition between logic “1” and “0” (see Fig. 5(a)). $I_p$ should be set to “0” during data nucleation to avoid leakage currents. After the data nucleation, $I_p$ is activated to induce domain wall motion in the magnetic stripe and we can obtain the same pattern at the read head MTJ1 after eight pulses (see Figs. 5(c) and 5(d)).
This simulation shows the correct operations of this PMA racetrack memory with low $I_w$ and $I_p$, allowing small die area (see Fig. 3). However, the operating frequency, 50 MHz is relatively low for advanced logic circuits, where a square wave is often used as the driving signal, (e.g., Clock), which can be generated more easily. Fig. 6 shows the transient simulation of this PMA racetrack memory with 500 MHz square wave $I_p$. To ensure both the domain wall nucleation ($\tau$) and motion (1 ns) in one cycle, current pulses $I_w \approx 414 \mu A$ and $I_p \approx 176 \mu A$ are, respectively, required. Note that it is difficult to use a 50% duty cycle square wave to drive the in-plane anisotropy racetrack memory as the duration of domain wall nucleation is much longer than that of domain wall motion.

Nevertheless, the higher currents allowing fast speed leads to larger die area. Fig. 7 shows the performance tradeoff of this racetrack memory in terms of power, speed and area. The X-axis corresponds only to the size of five MOS transistors for switching (see Fig. 3) as the sensing circuit is kept the same whatever the speed. $F$ is the feature size of technology node. Square wave $I_p$ pulse is used for all the simulations and the data storage speed is shown to be linearly increased up to 500 MHz with 40 $F^2$ die area. Assuming the area of sensing circuit $\approx 20 F^2$, one can briefly calculate cell area for our PMA CoFeB racetrack memory, which is about $60/8 = 7.5 F^2/bit$. If there are 64 constrictions in the magnetic stripe, the cell area would be nearly $1 F^2/bit$, smaller than other non-volatile storage technologies.

The energy dissipation per data storage operation $E_{RM}$ can be described by Eq. (10):

$$E_{RM} = V_w \times I_w \times D_w + V_p \times I_p \times D_p,$$

where $V_w$ and $V_p$ are the power supplies of current sources for domain wall nucleation and motion; $D_w$ and $D_p$ are the

FIG. 6. Transient simulation of PMA racetrack memory driven by 500 MHz square wave $I_p$. (a) Current pulse $I_w$ for switching the state of MTJ0. (b) Current pulse $I_p$ valued 176 $\mu A$. (c) State of read head MTJ1, the eighth storage element in the magnetic stripe. (d) State of write head MTJ0, following $I_p$ pulses, data are stored in series in the magnetic stripe.

FIG. 7. The dependence of $I_p$ current pulse frequency (blue solid line) and energy dissipation (black dotted line) versus CMOS die area for one 8-bit racetrack memory word.

FIG. 8. The dependence of energy dissipation and operating frequency versus racetrack memory technology node.
pulse durations of $I_w$ and $I_p$, which are both equal to $1/2T_p$ and $T_p$ is the period of the square-wave current pulse $I_p$. $E_{RM}$ can be advantageously lower than $\sim 1$ pJ, but it will be only slightly reduced for large die area, as shown in Fig. 7. This is due to the nearly linear relationship between both the DW nucleation and motion currents with duration (see Eqs. (6)–(8)). The potential power efficiency of this PMA race-track memory following feature size F minimization is also studied by using the compact model (see Fig. 8). F presents important impact on dissipated energy as the small size of racetrack memory reduces linearly the DW nucleation and motion currents while keeping the same delay (i.e., $D_w$ and $D_p$) or operating speed. Two frequencies 500 MHz (solid line) and 250 MHz (dotted line) have been simulated and Fig. 8 shows that about 75%–90% $E_{RM}$ can be saved with the shrinking of technology node from 65 nm to 15 nm.

**IV. CONCLUSION**

In summary, we present the first design of PMA race-track memory composed of a CoFeB magnetic stripe and two CoFeB/MgO/CoFeB MTJs. A spice-compatible compact model based on physical theories and experimental measurements has been developed to demonstrate its operations and high performance. According to the simulation results, extremely small area (e.g., $\sim 1$ F²/bit), fast-speed (e.g., 500 MHz), and low power can be expected beyond STT-MRAM, Flash and other non-volatile memory technologies. A PMA CoFeB racetrack memory prototype is under investigation in our laboratory.

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