High reliability sensing circuit for deep submicron spin transfer torque magnetic random access memory

Wang Kang, Weisheng Zhao, J.-O. Klein, Youguang Zhang, C. Chappert and D. Ravelosona

A high reliability offset-tolerant sensing circuit is presented for deep submicron spin transfer torque magnetic tunnel junction (STT-MTJ) memory. This circuit, using a triple-stage sensing operation, is able to tolerate the increased process variations as technology scales down to the deep submicron nodes, thus improving significantly the sensing margin. Meanwhile, it clamps the bit-line voltage to a predefined small bias voltage to avoid any read disturbance during the sensing operations. By using the STMicroelectronics CMOS 40 nm design kit and a precise STT-MTJ compact model, Monte Carlo simulations have been carried out to evaluate its sensing performance.

Introduction: Spin transfer torque magnetic tunnel junction (STT-MTJ) memory has emerged as a promising candidate for the next generation high-density, low-power and scalable non-volatile random access memory technology [1]. The MTJ nanopillar is mainly composed of three layers: one oxide barrier sandwiched between two ferromagnetic (FM) layers as shown in Fig. 1a. It presents two resistance values ($R_P$ or $R_R$) depending on the relative magnetisation orientations of the two FM layers. The resistance difference is characterised by the tunnel magneto-resistance ratio ($TMR = (R_P - R_R)/R_R$). A typical STT-MTJ bit cell consists of a MTJ connected in series with an access transistor between a bit-line (BL) and a source-line [2], as shown in Fig. 1b. Only a bidirectional spin polarised low current $I_{write}$ larger than a threshold value $I_{c}$ can switch the MTJ state, and a read current $I_{read}$ can be used to sense the MTJ state [1]. It is worth noting that $I_{c}$ should be sufficiently less than $I_{c}$ to avoid any read disturbance (RD) during the sensing operation. However, low $I_{c}$ leads to a small sensing margin (SM) accordingly due to the small TMR ratio and process variations. Therefore there exists a conflict, and it is of great importance to design the best trade-off between SM and RD for the sensing circuits. Conventional sensing circuits, such as the dynamic current-mode (DCM) sensing amplifier [3], the self-reference sensing scheme [4] and the pre-charge sensing amplifier (PCSAs) [5], cannot overcome the conflict between SM and RD. Moreover, they suffer from low reliability owing to the reduced supply voltage and increased process variations, as technology scales down to the deep submicron nodes (e.g. 40 nm). In this Letter, we propose an offset-tolerant triple-stage sensing circuit to tolerate the process variations and overcome the conflict between SM and RD.

**Fig. 1** Structure of STT-MTJ cell

a Vertical MTJ nanopillar structure
b Typical 1T1MTJ bit cell structure

Proposed sensing circuit: Fig. 2 shows the schematic of the proposed sensing circuit, which is mainly composed of two parts: a current converter and a comparator. One bit of information is stored in each data MTJ as $R_P$ or $R_R$. The reference cell is formed by paralleling two serially connected MTJs as shown in Fig. 2, and its resistance $R_{ref}$ equals ($R_P + R_R$)/2. The access transistors for both data and ref cells are with minimum feature size. The triple-stage sensing operation is detailed as follows. In the first stage, after a data cell is selected by enabling a word-line and a BL, a biasing voltage $V_{bias}$ is added to the operational amplifier $A_0$ of the current converter. The current flowing through the transistor $N_0$ is $I_{bias} = V_{bias}/R_{n0}$, here, $R_{n0}$ denotes the resistance of the selected data cell, which includes the resistance of both the MTJ $R_{m0}$ and the access transistor $R_{a0}$. Then, the voltage $V_a$ induced by the load PMOS $P_0$ ($P_0$ can be also replaced by a resistor $R_{col}$) is stored in the switched capacitor $C_0$ as $V_{ref}$ by enabling the switch gate $S_0$. In the second stage, we select a reference (ref) cell by enabling the ref-line and a ref-select-line. The current flowing through $N_0$ is $I_{ref} = V_{bias}/R_{ref}$, here $R_{ref}$ denotes the resistance of the selected ref cell, which includes the resistance of both the ref MTJs and the access transistor. Then the induced voltage is stored in the switched capacitor $C_1$ as $V_{ref}$ by enabling $S_1$. Finally, in the third stage, the $V_{data}$ stored in $C_0$ and the $V_{ref}$ stored in $C_1$ are connected to a differential latch-type comparator $A_1$, and the difference between $V_{data}$ and $V_{ref}$ is amplified to a digital signal ‘0’ or ‘1’. Since we use the same sensing path to generate both $I_{n0}$ and $I_{ref}$, we can eliminate the mismatch in the sensing circuit induced by the process variations, leading to offset-tolerant currents $I_{n0}$ and $I_{ref}$. The difference ratio between $I_{n0}$ and $I_{ref}$ is expressed as follows:

$$\frac{|I_{n0} - I_{ref}|}{I_{ref}} = \left| \frac{V_{bias}/R_{m0} - (V_{bias}/R_{ref})}{V_{bias}/R_{ref}} \right| = \frac{R_{ref} - R_{m0}}{R_{ref}} \quad (1)$$

The induced voltage $V_{data}$ and $V_{ref}$ can be further amplified by a suitable choice of $P_0$ or $R_{col}$, thus increasing the SM. The process variation or mismatch in the comparator is very small compared to the amplified SM and can be further reduced by optimising the switched capacitors and the amplifier $A_1$. Meanwhile, since we apply a small $V_{bias} \leq 0.1$ V at the current conveyor, the currents flowing through the data cell and ref cell are sufficiently small to avoid any RD. For example, assume $I_{c0} \approx 60 \mu A$, $R_{m0} \approx 4.5$ kΩ and $R_P \approx 3.5$ kΩ at 40 nm technology node, when the resistance $\times$ area $(R \times A)$ product is 5 Ω·μm² and the TMR ratio is 150%, respectively. Then the maximum current is $I_{bias} \approx 12.5$ μA, which is far less than $I_{c0}$.

Monte Carlo simulation: As discussed above, two parameters, i.e. TMR ratio and $V_{bias}$, have most important impacts on the sensing performance of the circuit. By using the STMicroelectronics CMOS 40 nm design kit [6] and a compact STT-MTJ model [7], Monte Carlo simulations have been performed. Here, we consider 3σ and 1% variations, respectively, for the CMOS transistors and STT-MTJs. Figs. 3a and 3b show the average SM and read current of the circuit with respect to TMR ratio and $V_{bias}$, respectively. The maximum read current is $I_{read} \approx 10.81$ μA and it leads to zero RD during the sensing operation. The total sensing time per bit is $\sim 4.3$ ns, including two 2.0 ns pulses for the data and ref cell sensing at the first two stages and $\sim 0.3$ ns for the third-stage amplifying. The total power consumption per bit sensing is $\sim 40.0$ Ω, composed of $\sim 35.0$ Ω for the first two stages and $\sim 5.0$ Ω for the third stage. Fig. 4 shows the sensing error rate of the proposed circuit compared to the DCM sensing amplifier [3] and the PCSA [5].
Conclusion: An offset-tolerant triple-stage sensing circuit for STT-MTJ memory is presented in this Letter. It tolerates the process variations and solves the conflict between SM and RD in deep submicron technology nodes. Monte Carlo simulations based on a 40 nm technology node are carried out to illustrate its high reliability performance.

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Wang Kang, Weisheng Zhao, J.-O. Klein, C. Chappert and D. Ravelosona (IEF, University Paris-Sud, CNRS, UMR8622, Orsay 91405, France)
E-mail: weisheng.zhao@u-psud.fr
Youguang Zhang (Electrical Engineering Department, Beihang University, Beijing 100191, People’s Republic of China)
Wang Kang: Also with the Electrical Engineering Department, Beihang University, Beijing, China

References