An Overview of Spin-based Integrated Circuits

Wang Kang\textsuperscript{1,2}, Weisheng Zhao\textsuperscript{1},*, Zhaohao Wang\textsuperscript{1}, Jacques-Olivier Klein\textsuperscript{1}, Yue Zhang\textsuperscript{1}, Djaafar Chabi\textsuperscript{1}, Youguang Zhang\textsuperscript{2}, Dafiné Ravelosona\textsuperscript{1}, and Claude Chappert\textsuperscript{1}

1, Institute d’Electronique Fondamentale (IEF), Univ. Paris-Sud, CNRS, Orsay, 91405, France
Tel : (+33)169156292
Fax : (+33)169154000
e-mail : weisheng.zhao@u-psud.fr

2, Electronics and information engineering, Univ. Beihang
Beijing, 100191, China
Tel : +86 01082314978
Fax : +81 01082339478
e-mail : kanebuaa@gmail.com

Abstract - Conventional CMOS integrated circuits suffer from serve power and scalability challenges as technology node scales into ultra-deep-micron technology nodes. Alternative approaches beyond charge-only based circuits. In particular, spin-based devices or integrated circuits show promising merits to overcome these issues by adding the spin freedom of electrons to the electronic circuits. Spintronics has now become a hot topic in both academics and industrials. This paper overviews the status and prospects of spin-based integrated circuits under intense investigation and address particularly their merits and challenges for practical applications.

I Introduction

Thanks to the good characteristics, such as high speed and small size, metal-oxide-semiconductor field-effect transistors (MOSFETs) and complementary MOS (CMOS) devices [1-3] (hereafter, both are referred to as MOS devices) are the fundamental technologies for mainstream integrated circuits. However the rapid and continual technology scaling progress of the MOS devices below 40 nm drives more and more issues and challenges, e.g., intrinsic leakage currents, dynamic power and process variability etc, indicating the end of MOS scaling in the near future [2, 3]. Many new advanced solutions, e.g., silicon on insulator (SOI) [4], have been proposed recently in order to alleviate this dilemma. They achieve one order of enhancement in some aspects, but they cannot overcome all the problems induced in the deep-micron technology nodes. In addition, the production cost including facility investment becomes very huge. Therefore alternative scaling-independent technologies, i.e., spin-based devices and circuits [5-7], for improving the integrated circuit performance have attracted considerable attention to sustain the Moore’s Law beyond the MOS scaling limit [2, 3]. Many research groups, including academia and industries are undergoing for this purpose.

Spintronics (or spin-electronics) is a rapidly emerging R&D area and it shows great promise in the future integrated circuits (both memory and logic computing) [5-7]. The basic concept of Spintronics is to control the spin property (besides charge) of electrons, as shown in Fig. 1, in ferromagnetic thin films based solid state nano-devices, such as spin-valve and magnetic tunnel junction (MTJ). It provides new concepts for future electronics, namely spin-based integrated circuits. The founding step of Spintronics triggered the discovery of the giant magneto-resistance (GMR) in 1988 (awarded Nobel Prize Physics 2007 for A. Fert and P. A. Grunberg) [8, 9], and soon triggered the definition of the spin-valve [10]. The spin-valve sensor was firstly commercialized by IBM in 1997 to replace the anisotropic magnetoresistance (AMR) sensor for hard disk drive (HDD) read heads and drove immediately the storage areal density growth rate of 100% per year. Another big step forward for Spintronics came from replacing the metallic spacer layer of the spin-valve with a thin non-magnetic insulating oxide layer (e.g., Al\textsubscript{2}O\textsubscript{3} or MgO), thus creating the magnetic tunnel junction (MTJ) [11-12]. In such configuration, much higher resistance difference, denoted as tunnel magnetoresistance (TMR) ratio, can be obtained at room temperature. The discovery of MTJ triggered intensive research and indicated a rapid development era on spin-based integrated circuits, such as magnetic random access memory (MRAM) and spin-transistors [5-7]. This paper overviews the status and prospects of the spin-based integrated circuits (including memory and logic circuits), and focuses mainly on the period after the discovery of the MTJ.

The rest of this paper is organized as follows: section II introduces the fundamentals of Spintronics. The spin-based memory and logic designs are described in section III and section IV respectively. Finally conclusions and perspectives are discussed in section V.

II. Fundamental of Spintronics

Spintronics is an emerging technology exploiting both the intrinsic spin degree of freedom and the magnetic moment of the electron, in addition to its fundamental electrical charge, in solid state devices. The origins of Spintronics can be traced back to the 1970s [13] and the research of Spintronics widely
emerged from the discovery of spin-dependent electron transport phenomena in solid-state devices in the 1980s [8, 9].

The discovery of spin valve or GMR in 1988 opens a new era in Spintronics, and later in 1995, the discovery of MTJ or TMR boosts its intensive research and applications [11, 12]. The MTJ nanopillar, as shown in Fig. 2, is one of the most important devices of current spin-based integrated circuits. Both perpendicular magnetic anisotropy (PMA) and in-plane shape anisotropy MTJs can be designed with different thin film composition.

The MTJ states, i.e., R_P or R_AP, can be switched by applying either a magnetic field or a spin polarized current. However conventional field-induced magnetic switching (FIMS) approaches [14] require writing current in the order of few mA to generate the required magnetic field and induce consequently high power consumption and hardware area. Much of academic and industrial research efforts have been focused on developing efficient strategies for switching the magnetization of the MTJ. One promising method relies on the spin transfer torque (STT), which was firstly proposed independently by Berger [15] and Slonczewski [16] in 1996, shows good performance. Only a small bidirectional current is required for the MTJ switching, which simplifies greatly the integration with the peripheral MOS circuits and therefore allows much higher density. Unfortunately according to the experimental measurements and theoretical models, the STT switching mechanism is normally stochastic (see Fig. 3 and Eqs. (2)-(5)) [17-19], thus resulting in reliability issues, which should be addressed in the practical spin-based applications.

Depending on the relative magnitude between the write current I_write and the critical current I_C0 (see Eq. (1)), the STT switching behaviour of the MTJ can be categorized into two regions: precessional switching region (I_write > I_C0) and thermal activation region (I_write < I_C0).

$$I_{C0} = a \frac{\gamma e}{\mu_B g} (\mu_0 M_s) H_K V = 2a \frac{\gamma e}{\mu_B g} E$$  \hspace{1cm} (1)

where a is Gilbert damping coefficient, $\gamma$ the gyro-magnetic constant, e the magnitude of the electron charge, $\mu_B$ the Bohr magneton constant, g the spin polarization efficiency factor, $\mu_0 M_s$ is the saturation field in the free layer, $H_K$ the anisotropy field, V the volume of the free layer and $E = (\mu_0 M_s)H_K V / 2$ is the barrier energy.

When the current flowing through the MTJ exceeds the critical current $I_{C0}$, the MTJ experiences a fast precessional switching regime, and the switching duration and probability can be expressed as,

$$Pr(t_{pulse}) = 1 - \exp \left( -\frac{t_{pulse}}{\tau_1} \right)$$  \hspace{1cm} (2)

$$\frac{1}{\tau_1} = \left[ \frac{2}{C + \ln (\pi \Delta t)} \right] \frac{\mu_B^P}{em(1 + P)} (I_{write} - I_{C0})$$  \hspace{1cm} (3)

where $t_{pulse}$ is the driver current pulse duration, $\tau_1$ is the mean duration for precessional switching regime, $C = 0.577$ is the Euler’s constant, $\Delta = E / k_BT$ is the thermal stability factor, $k_B$ the Boltzmann constant, $T$ the temperature, m the free layer magnetic moment, P the tunneling spin polarization of the ferromagnetic layers. Otherwise, if the current is lower than $I_{C0}$, the switching process can still occur with a long pulse thanks to the thermal activation. The switching probability and pulse duration for the thermal activation regime can be expressed as,

$$\frac{dPr(t_{pulse})}{(1 - Pr(t_{pulse})) dt} = \frac{1}{\tau_2}$$  \hspace{1cm} (4)

$$\tau_2 = \tau_0 \exp \left( \frac{E}{k_BT} (1 - \frac{I_{write}}{I_{C0}}) \right)$$  \hspace{1cm} (5)

where $\tau_0$ is the attempt period, $\tau_2$ the mean pulse duration for the thermal activation regime. In the practical spin-based integrated circuits, we generally require the MTJ operates at precessional switching regime and choose short pulse current with amplitude larger than $I_{C0}$ to get high speed operations.

The MTJ resistance states can be sensed with either a bias voltage $V_{bias}$ or a directional current $I_{read}$ due to the TMR effect. Generally a relative larger $V_{bias}$ or $I_{read}$ is required to improve the sense margin (SM). However it is worth noting that the sensed current or $I_{read}$ should be sufficiently less than $I_{C0}$ to avoid any read disturbance (RD) (see Eq. (6)) for the STT-based MTJ [19-21]. In addition, larger $V_{bias}$ may lead to TMR loss (see Eq. (7)) [21].

$$Pr_{dis}(t_{read}) = 1 - \exp \left( -\frac{t_{read}}{\tau_0} \right) \exp \left( -\frac{\Delta(1 - \frac{I_{read}}{I_{C0}})}{E} \right)$$  \hspace{1cm} (6)

$$TMR_{real} = \frac{TMR(0)}{1 + V_{bias}^2 / V_{k_BT}}$$  \hspace{1cm} (7)

where $I_{read}$ and $t_{read}$ are the amplitude and accumulated duration of the sensing current, TMR_{real} is the TMR ratio after adding bias voltage, TMR(0) is the TMR ratio with 0V
voltage, $V_b$ is the bias voltage as $\text{TMR}_{\text{real}} = 0.5 \times \text{TMR}(0)$.

The STT-based MTJ has been widely used and become the major candidate device, at least in the short term, in the spin-based integrated circuits. Many STT-MTJ based memory and logic circuits or prototypes have been presented in the last years, such as STT-MRAM and Magnetic Flip-Flop (MFF) etc. They show many great merits, such as high speed, low power, non-volatility and instant on/off capability, especially the good compatibility and scalability performance to continue the Moore’s scaling law.

III. Spin-based memory circuits

There are different methods to categorize these spin-based memory circuits. In this section, we will overview and classify them from the device structure point of view.

A. Spin-based HDD read head

Spin-valve sensor for HDDs [5], as shown in Fig. 4, utilized in 1997 by IBM, is the first commercialized application of Spintronics, which provides a sensitive and scalable read technique for HDD and brought huge economic interests. Both geometries, i.e., current in plane and current perpendicular to plane (CPP) were proposed, but the CPP geometry is much better for integration and achieving minimum dimension. In addition, the CPP configuration is also more favorable for reducing the recording track width. The spin-valve sensor increased the HDD areal recording density by three orders of magnitude (from ~0.1 to ~100 Gbit in $^2$) between 1997 and 2003. However, this growth rate started to slow down after 2003, when other problems joined the limiting spin-valve head. The MTJ read head, with the same structure as spin-valve shown in Fig. 4, except replacing the metallic spacer layer M with a thin non-magnetic insulating layer (e.g., Al$_2$O$_3$ or MgO), was then commercialized in 2004 by Seagate. The MTJ read head promises to achieve over 200 Gbit in $^2$ recording density and 1 Gbit/second data rate.

B. Magneto-resistive Random Access Memory (MRAM)

MRAM is mainly based on the hybrid structure, i.e., the magnetic memory elements (generally referred to the MTJ) integrated with the MOS devices. There exist two basic array architectures, i.e., one-transistor with one MTJ (1T-1MTJ) and cross-point architectures [5, 22-23]. In the 1T-1MTJ architecture, as shown in Fig. 5, each MTJ is connected in series with an MOS transistor, where the gate of the transistor is connected to the word-line (WL), drain to the bit-line (BL) crossing the MTJ and source to the source-line (SL). It is convenient for selecting the cell for the write/read operations. However the density of the 1T-1MTJ array architecture is less than the cross-point architecture due to the transistor required for each memory cell. In the cross-point array architecture, the MTJs lie at the intersection of the WLs and BLs, as shown in Fig. 6, where the pinned layer and free layer of the MTJ are connected directly to the BLs and WLs respectively. This arrangement allows for a considerable packing density, since no contact is made to the silicon die within the cell. However it involves several significant design challenges, such as low data access speed and sneak currents, leading to poor write/read performance.

The read operation of the MRAM utilizes a bias voltage on the BL to measure the effective current, or applies a current flowing through the cell to measure the voltage. There are three basic decision-making methods to determine the data value stored in the memory cell: the reference-cell method, complementary-cells comparison method and self-referenced method [23-26]. In the reference-cell method, each sensed value of the memory cell is compared to a reference cell, with resistance value $R_{\text{ref}} = (R_p + R_{\text{ref}})/2$. This method should be designed with consideration of the process variations, especially as technology scales down to the ultra-deep-micron

---

Fig. 4. The spin-valve read head for hard-disk recording. (Left) The schematic configuration of the ‘current in plane’ geometry; (Right) The ‘current perpendicular to plane (CPP)’ geometry [5].

Fig. 5. Schematic of MRAM structure [5]. (a) Data representation with different MTJ configurations; (b) Schematic of the MTJ cell structure; (c) Schematic of the 1T-1MTJ array architecture.

Fig. 6. Schematic of the cross-point architecture for MRAM [22].
technology nodes. The second method uses two MTJs, which are always written to opposite states, to store one bit of data. This method can improve greatly the sense margin (SM) compared with the first one, but with lower storage density. The self-referenced method accesses the memory cell twice, and makes the decision based on a known value written into the cell at the second time or based on the physical characteristics of the MTJ R-I curves. This method requires no hardware for the reference cells, and it is insensitive to process variations. However the repeated sense cycles result in considerable read latency and power consumption. In addition, it also leads to endurance reliability issues.

The write operation of the MRAM is different based on the writing mechanism of the MTJ, and we can classify the MRAM family into several categories as following (see also Fig. 7): (a) Field-induced magnetic switching (FIMS) MRAM; (b) Spin transfer torque (STT) MRAM; (c) Thermally-assisted switching (TAS) MRAM.

**FIMS-MRAM**

FIMS-MRAM [14] is the first generation of MRAM that based on the field-only writing mechanism, as shown in Fig. 7 (a), where the magnetic fields are generated by two orthogonal current lines. In such approach, the write selectivity is based on the combination of two perpendicular pulses of magnetic fields, i.e., \( H_x \) and \( H_y \), which may result in narrow write margin and half-selectivity issues. In addition, high power consumption (magnetic fields requiring write currents of about 7-10 mA) and poor scalability (selectivity problems caused by magnetic field dispersion) limit its commercialization. Later in 2003, the selectivity problem is solved by introducing a new write method, named toggle-switching [27], which is based on the use of a synthetic ferrimagnetic (SF) free layer and is commercialized in 2006 by Everspin. However this method needs to read before write and it also consumes high write power. Most importantly, the general downscale scalability problem (cell size about 30 F^2) with field writing mechanism cannot be well overcome.

**STT-MRAM**

STT-MRAM [16-17, 28], as shown in Fig. 7 (b), uses a bi-directional low current (~1-2mA/cm^2) to switch the MTJ, and this simplifies greatly the integration with the peripheral MOS circuits, thus achieving very good scalability (down to 10 nm diameter) and high integrated density (with minimum cell size of 6 F^2). The key challenge for STT-MRAM is to achieve low write current, high speed, good endurance as well as long retention simultaneously, because (a) both \( I_{CW} \) and the thermal stability factor \( \Delta \) is proportional to the barrier energy \( E \) (see Eq. (1) and (3)), there exists a conflict between low current and long retention; (b) to get high speed (i.e., short write duration \( t_{pulse} \)), a high write current \( I_{write} \) is required (see Eq. (3) and (5)), therefore a high bias voltage \( V_{bias} \) or low resistance.area product (R.A) is needed to achieve this purpose, as shown in Fig. 8. However, both the two solutions lead to the oxide barrier breakdown and thus poor endurance of the MTJ.

**TAS-MRAM**

To solve the dilemma between write performance and retention, and meanwhile to continue the MRAM downsize scalability, a new concept, named thermally assisted switching (TAS) was proposed [29, 30]. As shown in Fig. 7 (c) and (d), this approach uses firstly a current pulse flowing through the cell to heat temporarily the free layer of the MTJ above its magnetic ordering temperature by Joule dissipation, greatly reducing the required magnetic fields or STT current for the MTJ switching. Then a magnetic field or current is applied for the magnetic switching of the MTJ. Finally the cell is rapidly cooled down to the room temperature and the magnetization of the MTJ subsequently remains frozen in the new direction. In such technique, the switching field or current can be fixed whatever the size of the MTJ, allowing a largest integration density and resolving the selectivity problem (only the addressed MTJ is heated). Moreover, the MTJ was written at elevated temperature and stored/read at room temperature, ensuring a high thermal stability and long data retention.

MRAM is an emerging non-volatile random access memory technology under development since the 1990s and is still under intensive research. Many prototypes or chips have been proposed or commercialized in markets currently. We believe that MRAM will eventually become dominant for all types of...
memory due to its overwhelming merits, becoming a universal memory one day. In summary, we compare the performance of various MRAM families, as shown in Table I.

### Table I: Comparison of Various MRAM Technologies

<table>
<thead>
<tr>
<th>Technology</th>
<th>FIMS MRAM</th>
<th>STT MRAM</th>
<th>TAS-FIMS MRAM</th>
<th>TAS-STT MRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scalability</td>
<td>Poor (&lt;60 nm)</td>
<td>Very good (&lt;10 nm)</td>
<td>Good (&gt;40 nm)</td>
<td>The best (&lt;8 nm)</td>
</tr>
<tr>
<td>Min cell size</td>
<td>Large (~30 F²)</td>
<td>Very small (~6 F²)</td>
<td>Small (~10 F²)</td>
<td>The best (~4 F²)</td>
</tr>
<tr>
<td>Endurance</td>
<td>10¹⁶</td>
<td>10⁴⁶</td>
<td>10¹⁴</td>
<td>The best ~10¹⁴</td>
</tr>
<tr>
<td>Writability</td>
<td>Poor</td>
<td>Very good</td>
<td>Good</td>
<td>The best</td>
</tr>
<tr>
<td>Power</td>
<td>Very high</td>
<td>Low</td>
<td>High</td>
<td>The best</td>
</tr>
<tr>
<td>Latency</td>
<td>Very long (&gt;20 ns)</td>
<td>Short (&lt;10 ns)</td>
<td>Long (~10 ns)</td>
<td>The best (&lt;8 ns)</td>
</tr>
</tbody>
</table>

C. Domain-wall (DW) racetrack memory

The observation of the current-induced domain wall (DW) motion in magnetic nanowires triggered the 3D storage devices, i.e., racetrack memory (RM) [31-32], as shown in Fig. 9, which promises to offer ultra-high storage density by storing the data in a U-shaped nanowire normal to the plane of the substrate. Combining with the MTJ nanopillars as the read and write heads, good CMOS integrability and fast data access can be achieved. The first RM prototype fabricated on 90 nm node has been presented recently; however, it is based on the in-plane magnetic anisotropy in NiFe nanowires with intrinsic low energy barrier, leading to insufficient data retention. Recent progress demonstrates that the perpendicular magnetic anisotropy (PMA) materials (e.g., CoFeB) can further improve the storage density, access speed and power consumption of the RM. Nevertheless, many challenges should be addressed before this device can be used in industry. One of the key challenges to build RM is to avoid any pinning defects in the magnetic strips, because even one single pinning defect may prevent the DW motion of the whole track.

D. Advanced spin-based memories

With the continual academic and industrial progresses on Spintronics, some new advanced spin-based memory concepts, such as voltage-controlled (VC) MRAM [33], multi-level-cell (MLC) MRAM [34] and multi-terminal structures [35, 36] etc, are proposed recently. The VC-MRAM uses the electrical filed through a voltage to assist or accomplish the switching of the MTJ, resulting in lower power consumption. MLC-MRAM formed by modifying the free layer structure of the MTJ or by stacking multiple MTJs in parallel or series, can store multiple bits in one memory cell, thus doubling or tripling the storage density. The multi-terminal cell structures based on spin-orbit torque effect: spin-hall or Rashba, as shown in Fig. 10, can indeed provide some aspects of advantages, e.g., improved endurance by reducing the electrical stress on the oxide barrier, but they also induce some drawbacks, e.g., larger cell size due to the two access MOS transistors. In summary, all these advanced concepts are still far away to be considered as promising approaches for practical applications due to their maturities and technological feasibilities.

IV. Spin-based logic circuits

Classic computing model of microprocessor is based on the Von-Neumann architecture [37], as shown in Fig. 11 (a), which consumes both high static power (due to the volatile cache memories based on MOS devices) and dynamic power (due to the data traffic between the CPU core and the main memories), limiting its further downsize scalability. For instance, the power to access the memory for fetching the instructions and reading/writing the data (e.g. ~1 pJ/bit/mm) is much higher than that for performing logic operations (e.g. ~1 fJ at 22 nm node). Therefore the spin-based logic devices and circuits, such as hybrid MTJ/C莫斯 logic structures, all-spin logic devices and spin-based transistors [38-41] etc, are under intensive investigation. They are expected to bring the non-volatility into the MOS circuits and then allow them to achieve instant on/off operations (i.e., powered off when unused and retrieved instantly on active state), reducing
greatly the static power. In addition, thanks to the vertical structure of the spin-based storage devices (e.g., MTJ), they can be fabricated above the MOS circuits at the back-end process. This 3D integration structure [7], as shown in Fig. 11 (b), shortens greatly the data traffic distance between the memory and logic chips, thus accelerating greatly the logic computing speed and saving significantly the dynamic power. In the following, we will overview several spin-based logic devices and structures that draw much attention currently.

A. Hybrid MTJ/CMOS logic circuits

The hybrid MTJ/CMOS logic circuits are mainly based on the logic-in-memory structure [38, 39], as shown in Fig. 12. It is mainly composed of four parts: a sense amplifier (S.A) to evaluate the logic result, a non-volatile memory block (e.g., MRAM), a write circuit, and a volatile MOS logic block. This type of spin-based logic circuits is the most popular one currently and draws considerable attention due to its instant on/off capability, zero standby power, good compatibility with conventional computing architectures and easy integration with the existing MOS technology process. Many hybrid MTJ/CMOS circuits or prototypes have been presented in the past few years, such as magnetic flip-flop (MFF), magnetic full adder (MFA) and magnetic look-up table (MLUT) etc. However they also suffer from some challenges which should be addressed, e.g., the switching latency (several ns) of the MTJ is much larger than those of the conventional MOS logic circuits, which limits the computing frequency to the order of GHz. Another severe issue is the poor sense reliability caused mainly by the device mismatch (both MOS and MTJs devices) of the S.As and the intrinsic stochastic switching effects of the MTJs. Different from the memory circuits where complex error correction circuits (ECCs) can be employed [42], it is difficult to embed them in the logic circuits while keeping fast speed, low area and high power efficiency. Therefore the current efforts that concentrate on this topic are fast-access MTJ development, high-performance S.A design, low-cost and reliable integration process etc.

B. Domain wall based logic circuits

Besides memory circuits, domain wall (DW) motion in magnetic nanowires provides also the ability of logic designs. One of the demonstrations is to use geometry dependence of the DW motion to perform logic computation [43], which uses no MOS transistors and exhibits ultra-low power consumption. However, these circuits utilize magnetic field to drive the DW movement and have some critical shortcomings, such as low speed (<100 KHz), magnetic field dissipation, scalability and reliability issues etc, for practical applications. The current induced magnetic DW motion becomes an effective solution to overcome these issues [31-32]. An alternative design is based on the DW motion racetrack memory (RM), as shown in Fig. 13 is an example of a MFA circuit [44]. It employs also the general logic-in-memory structure to perform the logic computing operations. Unlike the hybrid MTJ/CMOS logic structure, where parts of the input data are volatile provided by the MOS circuits (see Fig. 12), in the DW motion based logic circuits, all the input and output data are stored in the non-volatile RMs, overcoming completely the standby power issue and achieving a real non-volatile logic circuit. However, all the data inputs are stored in non-volatile state, which is difficult to be realized with a reasonable area and latency overheads. In addition, it faces the same challenges (e.g., pinning defects) as introduced in the RM circuits.

C. All-spin logics

All spin logic devices (ASLD) [40], as shown in Fig. 14 (a), which employs nano-magnets as digital spin capacitors to store data information and spin currents (through spin transfer torque) to communicate, realizing logic gates based on the spin majority evaluation. As shown in Fig. 14 (b) is an example to demonstrate the possible layouts for constructing cascadable ASLD logic gates. The magnetization directions of the nano-magnets can be switched between the stable states if enough torque is exerted on them. Information stored in the input magnet is used to generate a spin current that can be routed along a spin-coherent channel to the output magnet, determining its state based on the spin transfer torque effect. The key feature of ASLD is its compactness and completeness, because no MOS transistor is needed for the logic operations and all the logic functions can be constructed with a minimal set of Boolean logic gates. With such design, a full spin
computing system can be expected with extremely low switching power. However this is still a theoretical prospect currently and many issues, such as reliability and clock control, are remaining unresolved. The most critical challenge for this ASLD is the “magic” material with strong spin orbit interaction and there are few experimental prototypes can produce successfully the theoretical results so far.

D. Spin-transistors

The concept of spin-transistor has been predicted early in the 1990s [45], but it was experimentally developed recently thanks to the rapid progress of ferromagnetic study on spin orbit interaction, and then a wide variety of spin transistors based on various operating principles have been proposed so far [46-47]. Spin-transistors, including “spin-MOSFET” and “spin-FET” devices, benefit from the similar structure as MOS transistors, as shown in Fig. 15. In the spin-FET and its related devices, the source and drain have the same spin alignment, and the on/off switching operation can be achieved by spin precession of the spin-polarized carriers injected in the channel through spin-orbit interaction. Here the spin-orbit interaction is controlled by the gate voltage. It is worth noting that particular channel materials with strong spin-orbit coupling, such as InGaAs, InAs and other III-V compounds, are required to sufficiently induce the spin-orbit interaction. However, the channel region of the spin-MOSFET requires a material with low spin-orbit coupling, since spin-MOSFET requires no spin precession of spin-polarized electrons in the channel. In the spin-MOSFET devices, the alignment of the drain magnetization is fixed, while that of the source can be changed, so the gate allows current to flow from the source to the drain without modulation. In contrast to the spin-FETs, the cutoff state of the spin-MOSFET is simply achieved by a gate bias condition in the same manner as an ordinary MOS transistor. In both type of devices, the spin is injected from the ferromagnetic source, and then transported through the channel to the drain and electrons with spin aligned with the drain are passed and generate current. Spin transistors provide a potential building element for novel integrated circuits and open a promising path for achieving real all-spin based integrated circuits.

E. Other spin-based logic devices and circuits

There are many other spin-based logic devices and circuits, such as spin-valve logic gates and graphene-based transistors etc [48-52]. Among them, graphene (awarded Nobel Prize in Physics in 2010 [51]) has been widely studied recently due to its ultra-high charge carrier mobility and long spin diffusion lengths, allowing it to be used as a promising channel material in the spin transistor. In 2008, the smallest graphene-based transistor was reported [50] to be successfully fabricated with only one atom thick and 10 atoms wide, and later in 2011, IBM announced that they had succeeded in creating the first graphene-based integrated circuit [52]. Graphene has proved generally the potentiality and capability of replacing silicon as a mainstream semiconductor. However many issues and challenges should be addressed before it can be widely used in industries. One of the key challenge is that single sheet of graphene is very hard to produce, and even harder to make on top of an appropriate substrate.

V. Summary and Conclusions

In this invited paper, we presented a general overview of the spin-based integrated circuits and addressed particularly its using as memories and logics by adding the spin freedom of electrons. The rapid progress in both physics and electronics makes them promising to overcome the power and scalability bottlenecks of conventional MOS-based integrated circuits, sustaining the Moore’s Law beyond the MOS scaling limit. Recently many prototypes or small-scale products have been successfully presented or commercialized, however many challenges should be relieved before they can be widely used in practical applications. For this purpose, many efforts have been done or are undergoing in both academics and industries. We believe that spin-based integrated circuits will become mainstream solution to build up the next-generation storage and computing systems.

Acknowledgments

This work was supported by ANR-DIPMEM, ANR-MARS, NVCPU projects and the CSC exchange program.

References


